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| **Program** | **: Computer Engineering** |  | **Year/Semester** | **: 2/IV A** |  |
| **Course (Course Code)** | **:** **Microprocessor Based System (MBS190806)** |  | **Period** | **: 24 Jan to 12 May 2023** |  |
| **Name of the Faculty** | **: Prachi Arora** |  | | | |

**TEACHING PLAN**

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| **Lecture**  **No.** | **Chapter Name, Sub topics and Teaching Points** | **Text book/ Ref book/ Web ref \*** | **Planned Date** | **Date of Implementation** | **Remark** |
|  | **CH 1 : The 8086 microprocessor** |  |  |  |  |
| **1** | **Introduction to Microprocessors:** overview of m/c level programs, assembly programs, role of processor in computer system, basic functions of processor, types of microprocessor, latest processors | **B1 : 2.2 – 2.10** | **27/1/23** |  |  |
| **2** | **Features of 8086:** Basic Features , Special Features , Miscellaneous Features | **B1 : 2.11** | **2/2/23** |  |  |
| **3** | **Architecture of 8086 – BIU and EU:** reason for 8086 architecture partition, explanation of BIU section of architecture – memory interface, physical address, logical address, physical address calculation formula, segment registers. | **B1 : 2.12 – 2.15** | **2/2/23** |  |  |
| **4** | **Architecture of 8086 – BIU and EU:** explanation of EU section of architecture – ALU, general purpose registers, explanation of 8086 architecture with example. | **B1 : 2.12 – 2.15** | **3/2/23** |  |  |
| **5** | **Flag register:** use of flag register,use of each flag bits with example. | **B1 : 2.12 – 2.15** | **9/2/23** |  |  |
| **6** | **Pin diagram of 8086:** Clock related pins, address-data de-multiplexed pins  **Instruction Queue:** concept of pipelining, Queue operations. | **L1** | **9/2/23** |  |  |
| **7** | **Memory of 8086:** memory banks **–** even and odd memory bank, access of even bank byte and word, access of odd bank byte and word. | **B4: 330-333** | **10/2/23** |  |  |
| **8** | **Memory of 8086:** memory segmentation, segment registers. | **B4: 330-333** | **16/2/23** |  |  |
|  | **CH 2 -** **Instruction set & timing diagram of 8086** |  |  |  |  |
| **9** | **Addressing modes of 8086:** Register addressing mode, immediate addressing mode, implied addressing mode, indirect addressing mode - register indirect addressing, resister relative indirect addressing. | **B2 : 112 - 127** | **16/2/23** |  |  |
| **10** | **Instruction types: Data Transfer group** : MOV, XCHG,XALT instruction, use, operation, example, flag related instructions – POPF,PUSHF | **B3 111** | **17/2/23** |  |  |
| **11** | **Arithmetic group :**  **Addition** – ADD, ADC, INC, DAA,AAA instruction use, operation, flags affected, example  **Subtraction** - SUB , SBB, DEC, NEG, CMP, DAS instruction use, operation, flags affected, example | **B3 156** | **23/2/23** |  |  |
| **12** | **Multiplication :** MUL,IMUL  instruction use, operation, flags affected, example  **Division :** DIV, IDIV  instruction use, operation, flags affected, example | **B3 156** | **23/2/23** |  |  |
| **13** | **Bit manipulation:**  **Rotate instructions** – ROL, ROR, RCL,RCR instruction use, operation, flags affected, example  **Shift Instructions –** SAR,SAL,SAR instruction use, operation, flags affected, example  **Logical instructions –** AND,OR,NOT,TEST,XOR instruction use, operation, flags affected, example | **B4 136 - 194** | **24/2/23** |  |  |
| **14** | **Program Transfer Instructions :**  **Jump instructions –** conditional jump instructions, unconditional jump**,** CALL and RET instruction. | **B4 136 - 194** | **2/3/23** |  |  |
| **15** | **String Instructions :** MOVS,LODS,CMPS,SCAS,STORS use of an instruction, operation, examples, program based on string instructions. | **B4 136 - 194** | **2/3/23** |  |  |
| **16** | **Stack instructions:** PUSH and POP instruction  **Process control instructions** : WAIT,HALT,TEST,NOP | **B4 136 - 194** | **3/3/23** |  |  |
|  | **CH – 3 8086 system bus structure** |  |  |  |  |
| **17** | **Signals for modes of 8086 :** Minimum & Maximum mode signals  **Clock generator 8284** – block diagram and working  **Bus controller 8288** – working | **B4-316** | **9/3/23** |  |  |
| **18** | **Modes of 8086 – minimum and maximum**  Use of minimum mode signals, diagram of minimum mode, details of each block, working process of minimum mode. | **B4 – 334, B3: 323-325** | **10/3/23** |  |  |
| **19** | **Timing diagram of minimum mode** – T-state, machine cycle, instruction cycle, IO Read/write, Memory Read/Write | **B4 – 334, B3: 323-325** | **16/3/23** |  |  |
| **20** | **Modes of 8086 – minimum and maximum**  Use of maximum mode signals, diagram of maximum mode, details of each block, working process of maximum mode. | **B4 – 334, B3: 323-325** | **16/3/23** |  |  |
| **21** | **Coprocessor 8087** – coprocessor concept, use of 8087, working and interfacing of 8087 with 8086. | **L2** | **17/3/23** |  |  |
| **22** | **Multiprocessor system** - Bus arbitration - Closely coupled and loosely coupled – Daisy chaining method, polling method, independence request method  **IO programming :** IN and OUT instruction | **L1** | **23/3/23** |  |  |
|  | **CH 4 - Interrupt structure of 8086** |  |  |  |  |
| **23** | **Introduction to Interrupts :** use of an interrupt, difference between polling and interrupt | **B3 - 451** | **23/3/23** |  |  |
| **24** | **Types of interrupts -** H/W v/s S/W, maskable v/s non maskable , vectored v/s non vectored, internal v/s external | **24/3/23** |  |  |
| **25** | **ISR** : interrupt service routine, process to execute an ISR of an interrupt.  **IVT :** Interrupt Vectored table, use of IVT, process to fetch the vectored number and ISR address. | **31/3/23** |  |  |
| **26** | 8086 interrupt structure, interrupt control instruction | **6/4/23** |  |  |
| **27** | Interrupt priority structure | **6/4/23** |  |  |
| **28** | **Feature**s and requirement of 8259 IC | **13/4/23** |  |  |
| **29** | **Architecture of 8259 PIC**, explanation of each block | **13/4/23** |  |  |
| **30** | Single Interfacing of 8259 with 8086 , overview of cascaded mode. | **13/4/23\*** |  |  |
|  | **CH 5 - Programmable devices** |  |  |  |  |
| **31** | **The 8255** **programmable peripheral interface** – need of 8255 PPI, handshaking concept, transfer using 8255 | **B5 : 149 -177** | 15/4/23\* |  |  |
| **32** | **Architecture of 8255 : introduction and use of** Port A, Port B, Port C, use of CWR (control word register) | **B5 : 149 -177** | 15/4/23\* |  |  |
| **33** | **Addressing of 8255 :** addressing for all ports and control word register, commands of 8255 : IO Command and BSR Command, example based on addressing and commands | **B5 : 149 -177** | 19/4/23\* |  |  |
| **34** | **Interfacing of 8255 with 8086:** operating modes of 8255 , programs based on interfacing of 8255 with 8086 | **B5 : 149 -177** | **20/4/23** |  |  |
| **35** | **Introduction to 8237 DMAC :** Requirement of 8237 DMAC, pin diagram | **B5 : 398** | **20/4/23** |  |  |
| **36** | **Architecture of 8237 :** block diagram and working of each block. | **B5 : 398** | **21/4/23** |  |  |
| **37** | Registers and operating modes of 8237 | **B5 : 398** | **21/4/23\*** |  |  |
| **38** | Interfacing and programming of 8237 with 8086 | **B5 : 398** | **27/4/23** |  |  |
|  | **CH 6 - Microprocessor application programs** |  |  |  |  |
| **39** | Basic interfacing concept, interfacing factors for 8086 | **B5 : 149 -177** | **27/4/23** |  |  |
| **40** | Working of seven segment display device.  Interfacing of 7 Segment display device | **B5 : 149 -177** | **28/4/23** |  |  |
| **41** | Basics of A/D and D/A  Interfacing of A/D converter and D/A converter | **B5 : 149 -177** | **28/4/23\*** |  |  |
| **42** | Temperature Controller | **B5 : 149 -177** | **4/5/23** |  |  |
| **43** | Traffic Light Control | **B5 : 149 -177** | **4/5/23** |  |  |
| **44** | Working of stepper motor  Stepper Motor Control | **B5 : 216** | **11/5/23** |  |  |
|  | **CH 7 -Introduction to Intel Pentium Architecture** |  |  |  |  |
| **45** | Features of Pentium processor. | **B4 - 716** | **11/5/23** |  |  |
| **46** | Pentium Superscalar architecture. | **11/5/23\*** |  |  |
| **47** | Pipelining. | **12/5/23** |  |  |
| **48** | Branch Prediction.  Instruction and Data cache. | 12/5/23\* |  |  |

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| **NAME & SIGNATURE OF FACULTY** | **SIGNATURE OF HOD** |  |  |  |  |  |  |  |  | **SIGNATURE OF PRINCIPAL/ VICE PRINCIPAL** |  |  |  |  |
| **Date ** |  |  |  |  |  |  |  |  |  |  |  |  |

\*extra lecture

**List of the Books:**

B1: Microprocessors and Interfacing, Douglas V. Hall

B2: The 8086 Microprocessor: Programming & Interfacing the PC, Kenneth J. Ayala

B3: The INTEL Microprocessors, Architecture, Programming and Interfacing, Barry B. Brey, Pearson Publishers

B4 : The 8088 and 8086 Microprocessors, Triebel, Walter A.,Singh, Avtar, Pearson Publishers

B5 : Advanced Microprocessors & Peripherals, By BHURCHANDI, A K Ray.

L1: <http://ece-research.unm.edu/jimp/310/slides/8086_IO1.html>

L2: <https://www.ques10.com/p/10902/explain-interfacing-of-8087-co-processor-with-8086/>